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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,166	10/06/2003	Naoyuki Tamura	243650US2S	5718

22850 7590 03/16/2007  
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.  
1940 DUKE STREET  
ALEXANDRIA, VA 22314

EXAMINER
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SIEK, VUTHE

ART UNIT	PAPER NUMBER
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2825

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/16/2007	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/16/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/678,166	<b>Applicant(s)</b> TAMURA ET AL.	
	<b>Examiner</b> Vuthe Siek	<b>Art Unit</b> 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,7,10,11 and 13-116 is/are rejected.
- 7) ☒ Claim(s) 6,8,9,12,17,18 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/6/03</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to application 10/678,166 filed on 10/6/2003.

Claims 1-23 remain pending in the application.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 10-11, 13-16, 19, 20 and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Teig et al. (7,155,697 B2).

4. As to claims 1 and 15, Teig et al. teach a method for compressing a semiconductor integrated circuit (IC) comprising dividing a design region, in which a semiconductor IC is to be designed, into a plurality of blocks; assigning semiconductor devices to each of the blocks, where circuit modules or circuit devices are placed or assigned within the blocks (col. 2 lines 17-29; Fig. 5 shows dividing an IC design into plurality of blocks (slots); determining a device density of each block (col. 8 lines 9-67; col. 9 lines 42-59); compressing any block that is determined to have a low device density (col. 2 lines 17-29; the compaction, which compresses the layout to decrease the total IC area meaning that the compression or compaction must be done on a low dense block); and connecting the blocks by wiring (col. 2 lines 17-29; Fig. 5).

5. As to claims 2-3, the limitations of assigning functions to the respective blocks by functional descriptions; and obtaining standard cells by synthesizing the function descriptions and obtaining standard cells by synthesizing the function descriptions are known and inherently within the art, since Teig teach assigning or placing circuit modules within the partitioned blocks (Fig. 5). The circuit modules are synthesized from circuit descriptions to perform functions. As shown in Fig. 5 each of the circuit modules or circuit devices assigned to partitioned blocks comprising standard cells.

6. As to claim 4, Fig. 5 shows circuit modules or circuit devices are assigned or placed with the partitioned blocks. Since the circuit modules or circuit devices placed or assigned to separate partitioned blocks or slots, they can be optimized separately within the partitioned blocks.

7. As to claim 5, Teig et al. teach EDA applications to recreate IC layouts comprising various geometric sizes and shapes representing the circuit modules to be designed on the partitioned block as shown for example in Fig. 5 (col. 1 lines 50-64). The geometric sizes and shapes of the circuit modules to be designed within the partitioned blocks clearly teach a custom layout.

8. As to claims 7 and 16, Teig et al. teach EDA applications to recreate IC layouts comprising various geometric sizes and shapes representing the circuit modules to be designed on the partitioned block as shown for example in Fig. 5 (col. 1 lines 50-64). Fig. 5 shows that even the positions of the circuit blocks (devices) are shifted within the block (slot), a wiring delay due to the shift does not affect an operation of the

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semiconductor IC because the functionality of the circuit blocks or devices does not changed.

9. As to claims 10 and 19, Teig et al. teach compressing of the block including reducing the size of a block with a low device density (col. 2 lines 17-29).

10. As to claims 11 and 20, Teig et al. calculating routing path capacities (wiring density) (col. 34 lines 43-67; col. 36 lines 6-67; col. 38 lines 29-67). Teig et al. teach a path is at risk if the estimated congestion (path-use plus blockages) is near or over the path's capacity (wiring density is found to be equal or higher than a predetermined density value) (col. 40 lines 57-67).

11. As to claims 13-14 and 22-23, Teig et al. teach a layout of circuit modules can have various sizes and shapes (col. 1 lines 50-63) depending on aspect ratios (col. 11 lines 55-67; col. 12 lines 1-50). The various sizes and shapes would be used to accommodate a required shape of an entire design (a compression ratio).

***Allowable Subject Matter***

12. Claims 6, 8, 9, 12, 17, 18 and 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest the claimed limitations as recited when incorporated with the base claims.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

  
VUTHE SIEK  
PRIMARY EXAMINER